### Features

Virtex 4, XC4VLX100-FF1513 FPGA

Compact PCI plug-in format (3U 4HP, 32/64 bit, 33/66MHz )

On-board memory interfaces:
- FLASH prom
- SODIMM socket for SDRAM
- SRAM via memory expansion

Debug Support Unit interface (RS232)

Memory expansion connector

User I/O Connectors (152 user i/o's)

Ethernet PHY 10/100 transceiver

On-board oscillators

ISP FPGA configuration via JTAG or Slave Serial interface

Specially designed and configurable for LEON core implementations

Capable of supporting LEON-FT core implementations

PIO expansion with 2 x RS232 / 2 x RS422 / 2 x LVDS options

### Description

The GR-CPCI-XC4V board is a Compact PCI format development board which has been developed in cooperation with Gaisler Research ([www.gaisler.com](http://www.gaisler.com)) especially to support the early development and fast prototyping of LEON systems. Although suitable for general purpose Virtex 4 designs, the incorporation of on-board volatile and non-volatile memory interfaces, together with serial and ethernet interfaces makes this board ideal for implementing LEON designs.

The LEON processor is a synthesisable VHDL model of a 32-bit processor compliant to the SPARC V8 architecture. It is provided in full source code under the GNU LGPL license, allowing free and unlimited use in both research and commercial applications.

This board, incorporating a Xilinx Virtex 4™ field programmable gate array, is capable of operating either as a stand-alone board, or as a compact PCI plug-in card in either the System slot or Peripheral slots.

Additionally, the design of this board can support the implementation of LEON-FT fault-tolerant systems if the implemented core incorporates these features.
Specifications

XC4VLX100-10FF1513C Xilinx Virtex 4 FPGA (standard option)

Typical core speeds 50 to 75MHz (depending on speed grade and core configurations)

On-board FPGA configuration proms

Memory and User I/O expansion using 120 pin and 60 pin connectors (AMP 177-984-5 and -2), for mezzanine card applications

Standard memory options:
- FLASH 128Mbit (4M x 32 bit)
- SDRAM SODIMM socket (up to 32M x 64 bit)
- SRAM via Memory Expansion connector and Mezzanine board

RJ45 10/100Mbit ethernet connector

SUB-D9 pin connector for DSU/UART I/F

(other options/configurations on request)

Applications and Support

The LEON processor is a synthesisable VHDL model of a 32-bit processor compliant to the SPARC V8 architecture which has been developed by Gaisler Research.

The source code availability and extensibility makes the processor ideal as the basis for small instruments, computer peripherals and as a general purpose controller or computing engine.

For more information on the LEON core, the VHDL model, synthesis, configuration, hardware and software development tools, IP core developments and technical support for the Leon processor, please refer to the Gaisler Research home page. (www.gaisler.com).

To support the early development and fast prototyping of LEON processor systems, Pender Electronic Design provides design support and hardware development boards. For more information please refer to the Pender Electronic Design home page (www.pender.ch).

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